WHAT WE CLAIMED ARE:

1. A power MOSFET device with reduced snap-back and being capable of increasing avalanche-breakdown current endurance, which has sequentially a drain with N^+ silicon substrate, an N^- epitaxial layer formed on said N^+ silicon substrate, a source contact region formed of N^+ doped well and P^+ doped well implanted after etching in a P^- well formed on said N^- epitaxial layer, and a gate electrode with deposition of polysilicon above a channel region between said N^- epitaxial layer and N^+ source contact region, said device is characterized in that: Said source contact region is formed by etching into said P^- well first and implanting P^+ dopant to the interface between said N^- epitaxial layer and P^- well, and the source contact region of said N^+ well and that of said P^+ well are not at the same level, by which it is possible to increase the avalanche-breakdown current durable capability of the power MOSFET device.

2. A method of manufacturing a power MOSFET device with reduced snap-back and being capable increasing avalanche-breakdown current endurance, comprising the following steps:

1. An N^- epitaxial layer is epitaxially grown on a N^+ silicon substrate;

2. A field oxide is grown on said N^- epitaxial layer;

3. Etching said field oxide and growing a gate oxide layer;

4. Depositing a polysilicon layer;

5. Performing photo masking and etching said polysilicon layer to form a polysilicon gate, and implanting and driving-in P^- dopant to form a P^- well;

6. Applying photo mask of N^+ dopant and implanting N^+ dopant to form a N^+ source;

7. Producing a photoresist, and after the source region is etched, implanting P^+ dopant to form a P^+ well, and subsequently removing the photoresist;

8. Depositing BPSG (Boro-Phosopho Silicate Glass); and

9. Performing a metalization of said source contact and processing the back contact of wafer to form a drain contact.